Automotive Qualification Plan Summary for LFCSP_SS at STATS ChipPAC China Jiangyin

TEST	SPECIFICATION	SAMPLE SIZE	EXPECTED COMPLETION DATE
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	3 x 77	June 2016
Solder Heat Resistance (SHR)*	JEDEC/IPC *J-STD-020*	3 x 11	June 2016
Highly Accelerated Stress Test (HAST)*	JEDEC *JESD22-A110*	3 x 77	June 2016
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC *JESD22-A118*	3 x 77	June 2016
High Temperature Storage (HTS)	JEDEC *JESD22-A103*	1 x 77	June 2016
Electrostatic Discharge *Field Induced Charge Device Model*	JEDEC *JESD22-C101*	3/voltage	June 2016

* These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125ºC; 2. Soak – unbiased soak for 192 hours at 30ºC, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260ºC. TC samples will be subjected to wire-pull test after 500 cycles where results should be within specification limits.